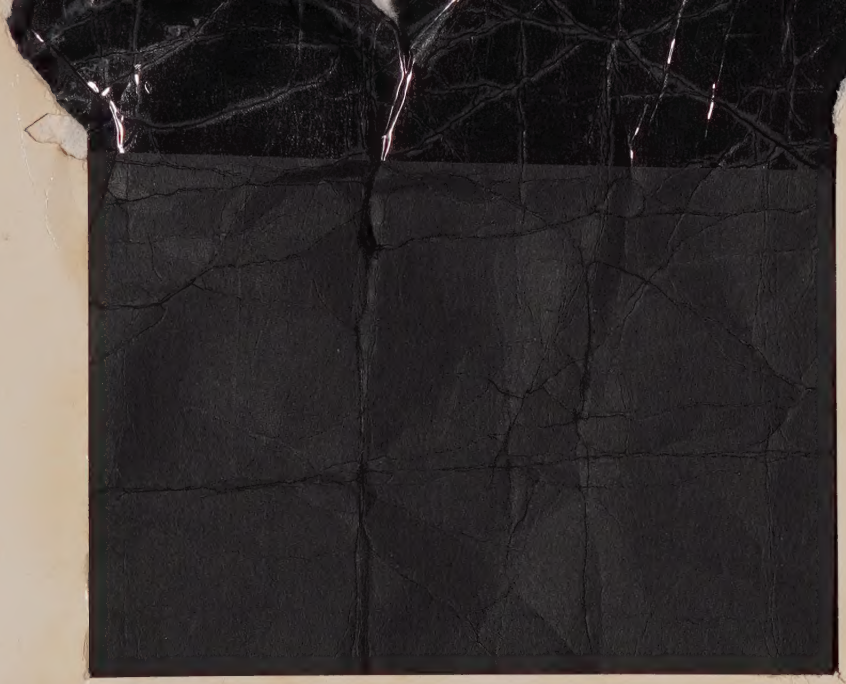

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Amendment Record

Incorporation of an Amendment in this publication is to be recorded by signing in the appropriate column and inserting the date of making the amendments.

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SECTION 1

Introduction

1.1—GENERAL

The counter-timer is a six-digit three-channel instrument covering the frequency band DC-50MHz. The instrument measures frequency, single and multi-periods, time intervals (single and double line working), pulse time, ratio and totalise.

All controls are available at the front panel with " gate open " and " overflow " indicators to give the operator instant visual reference.

A 10MHz high stability crystal oscillator provides the timebase reference for all time and frequency measurements.

1.2—APPLICATIONS

The frequency band covered, together with the range of functions offered, allow the SL114 to meet most laboratory counter timer applications. The pulse response and wide range of input facilities also allow this instrument to tackle a large number of different types of timing measurements in industrial, research and educational programmes.

1.3—OPTIONAL FEATURES

Optional facilities include B.C.D. output, rack mounting, and 8-digit display. The design also anticipates special customer options and the PCb layout ensures easy application of these further requirements.

SECTION 2

Technical Specification

Frequency Measurement Channel " A "

Select Function, " Frequency " and Channel " A "

Frequency Coverage:

20 Hz — 99.9999 KHz
20 Hz — 999.999 KHz
20 Hz — 9999.99 KHz
100 Hz — 50.0000 MHz
1 KHz — 050.000 MHz
10 KHz — 0050.00 MHz
100 KHz — 00.0500 GHz
1 MHz — 000.050 GHz
10 MHz — 0000.05 GHz

Input Sensitivity: 10mVrms 20 Hz to 20MHz, 50mVrms to 50MHz } Typical

Input Impedance: Approx. 1MΩ in parallel with 30 pF

Maximum Input Level: 400v DC 250v AC @ 50-600Hz. Decreasing at higher frequencies.

Coupling: AC

Attenuator: 20 db.

Filter: Low Pass

Frequency Measurement Channel " B " and " C "

Select Function, " Frequency " and Channel " B " or " C "

Frequency Coverage:

0.1 Hz — 99.9999 KHz
1 Hz — 999.999 KHz
10 Hz — 9999.99 KHz
100 Hz — 10.0000 MHz
1 KHz — 010.000 MHz
10 KHz — 0010.00 MHz
100 KHz — 00.0100 GHz
1 MHz — 000.010 GHz
10 MHz — 0000.01 GHz

Input Sensitivity: 100mV rms.

Maximum Input Level: 400v DC 250v AC @ 50-600Hz. Decreasing @ higher frequencies.

Input Impedance: Approx. 1MΩ in parallel with 30 pF

Pulse Duration: ≦ 50ns minimum at trigger points.

Coupling: AC or DC.

Attenuator: 20 db.

Filter: Low pass.

Period Measurement

Select Function " Period " and Channel "A," " B " or " C "

Input: See appropriate channel specification given in " frequency measurement."

Clock Unit: 0.1 μsec.

Periods Averaged: 1 to 10^3 in decade steps.

Range: 0.001 ps to 100 ms.

Coupling: AC or DC.

Totalizing

Select Function "Total ÷ N " and Channel " A," " B " or " C "

Input:	See appropriate channel specification given in frequency measurement.
Coupling:	AC or DC.
Maximum Rate:	50 x 10^6 events per second.
Prescaling:	Events may be prescaled in decade steps from 1 to 10^3 (N).
Display:	$\frac{\text{Number of input events.}}{(N)}$
Manual Start/Stop:	Front panel push-buttons. Successive operation of the start/stop buttons allows accumulation of events
Electrical Start/Stop:	By TTL logic level " O " or contact closure to common line applied to start/stop inputs.
Reset:	Front panel push button or TTL logic level " O " or contact closure to common line will clear display.

Ratio Measurement

Select Function " Ratio $\frac{A}{B}$ × N "

H.F. Input:	Channel "A" AC coupled.
Frequency Range:	20 Hz to 50 MHz.
L.F. Input:	Channel ' B " DC coupled.
Frequency Range:	DC to 10 MHz.
Display:	Frequency $\frac{\text{"A"}}{\text{"B"}}$ × N.
Multiplier (N):	1 to 10^3 in decade steps.

Time Interval

Select Function "Time Interval A ▸ B"

Input:	Channel " B " ▶ " C." '
Coupling:	DC.
Clock Units:	0.1 μs.
Input Channel.	Start channel " B." Stop channel " C."
Trigger Slope:	Positive/negative edge and level selection.
Range:	0.1 ns x 1.0 10.0
	0.1 ms x 1.0 10.0
	0:1 sec x 1.0 10.0

Frequency Standard

Frequency:	10 MHz.
Temperature Stability:	Better than 5 parts in 10^7 per 0-50 °C.
Average Ageing.	Better than ±5 parts in 10^7 per month, decreasing with age to typically 1 part in 10^7 per year after approximately 1 year continuous use.

Power Supplies

Voltage:	100-120v, 210-250v in 10v increments.
Frequency:	50-400 Hz.
Power:	Approximately 36 VA.

Dimensions

Width:	33cm. (12.9ins.).
Height:	9cm. (3.5ins.).
Depth:	29.5cm. (11.6ins.).
Weight:	3.2kgm. (7lbs.).

Options

01 B.C.D. Output.
02 Rack Mounting Kit.
04 Extra Two Digit Display.

The company reserves the right to change this specification if necessary without further notification.

SECTION 3

Operating Instructions

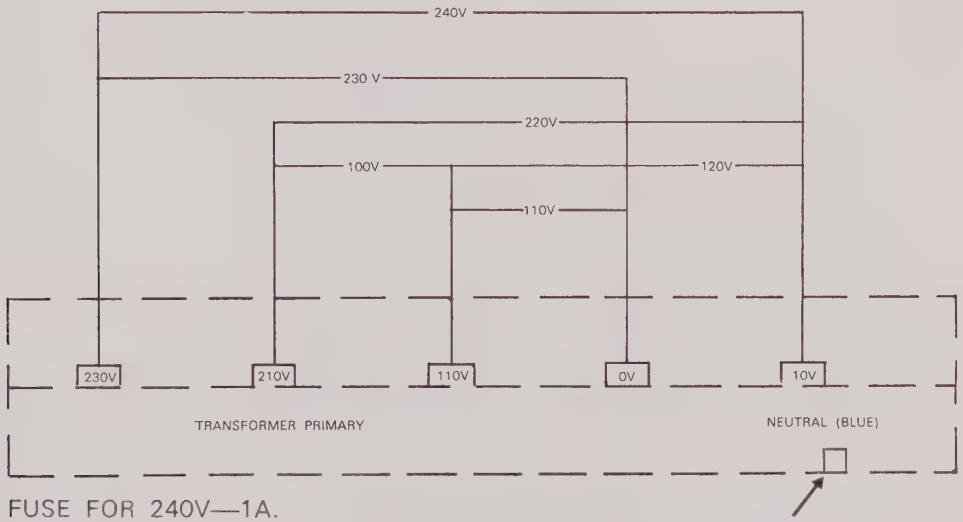
3.1—CONNECTING THE SUPPLY

Before connecting the supply to the counter check that the mains plug is wired in accordance with the regulation for supply connections.

BROWN ..... LIVE
BLUE ..... NEUTRAL
GREEN/YELLOW ..... EARTH

The unit is normally connected for 240V a.c. operation. If the supply is not 240V a.c. refer to the diagram below for alternative selection.

NOTE: Fuse rating must be changed when selecting the lower input voltage ranges of 110V typical, and the unit must be unplugged from the supply source for any alterations to the primary wiring.



FUSE FOR 240V—1A.
FUSE FOR 110V—2A.

Spare tag, this may be in a different position.

3.2—SUPPLY CONTROL

The supply to the instrument is controlled by the power switch which has three positions.

POSITION 1 — This is the " USE " position for bench and laboratory operation.

POSITION 2 — This is the power " OFF " position.

POSITION 3 — This is the " STANDBY " position with power removed from the display but all other systems fully operational. Thus, this feature is used for system or automatic control using the B.C.D. option.

3.3—COUNTER/DISPLAY CONTROL

(i) **Gate Open Indicator** This light emitting diode glows whenever the input to the display decade counters is enabled.

(ii) **Store Toggle Switch** This switch controls the transfer of display counter information via the store to the display. The display may either show the contents of the display counter as it counts (non store) or the result of the last count whilst performing a new cycle (stored).

(iii) **Display Time Control** At the end of any count sequence (except TOTAL), the time for reading the resultant display count before internally resetting may be adjusted between less than 200ms to greater than 5s by the Display Time Control. With the control turned fully anticlockwise until the switch operates, the display counter will be held until the unit is switched off or the reset button is pressed.

3.4—INPUT CHANNEL AMPLIFIERS

"A" Channel

The "A" channel is 20Hz-50MHz a.c. coupled with an input impedance of 1Mohm.
This channel will accept very low input levels of less than 10mV rms to 20MHz rising to 50mV rms at 50MHz.
A 20db attenuator and an HF filter are incorporated where high level or low level signals in electrically noisy industrial environments are encountered.
When the test button is used the incoming signal to the "A" channel is disconnected from that amplifier and a low level signal derived from the internal oscillator at 10MHz is substituted. This provides a simple check facility in the " FREQ," " PERIOD " and " TOTAL " modes. Also included is a trigger level control to ensure reliable triggering at low level inputs and enable trigger level selection where noisy signals are encountered.

"B" and "C" Channels

The " B " and " C " channels are identical a.c./d.c. coupled amplifiers with an upper frequency limit of 10MHz. The sensitivity is 100mV rms and each channel has its own HF filter and 20db attenuator for use in electrically noisy environments.
The trigger level controls and slope switches on each channel simplify the precise measurement of time intervals.
To further assist in the measurement of pulse timing, a " B " and " C " " COM " switch is incorporated which connects the " B " and " C ' input amplifiers to the " B " channel input socket and isolates the " C " channel input socket.

3.5—INPUT CHANNEL AND FUNCTION SELECTION

The input channel selection switch is used to route the appropriate input amplifier to the control logic in the " FREQ," " PERIOD " and " TOTAL " mode of the function switch. In the other positions " RATIO " and " TIME B▶C " the routing is automatic with function selection.

3.6—DECIMAL POINTS AND UNITS INDICATORS

The decimal points are automatically operated in the "FREQ" and "PERIOD" modes and they are selectively positioned by the timebase switch.
The units indicators are automatically operated in the " FREQ " and " PERIOD " modes and are selected by the multiplier switch.

3.7—OVERFLOW INDICATOR

Whenever the most significant digit (LH) changes from a 9 to a 0 during a counting sequence, the overflow indicator will glow to indicate that the count during the measurement was greater than the maximum count shown in the decades provided. Overflow status is automatically cleared every internal and external reset.

3.8—TIMEBASE/MULTIPLIER

The timebase/multiplier switch routes the input and outputs of eight decade dividers to provide division ratios in three ranges, each with three multiplier positions.

X1		X1
X10	×	$X10^3$
X100		$X10^6$

Thus, to obtain $X10^4$ it is necessary to depress X10 and $X10^3$ or to obtain X100 the X100 and X1 switch is depressed.
These ranges give divisions from 1 to 10^8 in timebase to allow the maximum timing facilities.

The divider chain is used to divide down from the 10 MHz clock frequency to operate the gate generator in the "FREQ" mode, and then as a period counter in the " MULTI/PERIOD " mode, and as a decade pre-scaler in the totalise mode.

It is also used as a multiplier in the " RATIO " mode and a time increment divider in the "TIME" mode. In this latter mode, time increments of 0.1 μs to 10s in the least significant digit position of the display are achieved.

SECTION 4

Modes of Operation

See Fig. 1 showing front panel controls

4.1—FREQUENCY MODE "A," "B" OR "C"

The signal applied to input "A" "B" or "C" may be sine wave, square wave, pulse, etc., of positive, negative or alternating polarity with respect to ground. Using the trigger level control, the trigger level may be set to any positive or negative value over a wide range, ensuring consistent triggering. The resulting output waveform is fed to the main gate, which is controlled by the clock and recycle oscillators.

The 10 MHz clock output is divided to produce timebase pulses, one of these time base pulses opening the main gate and the next closing it. When the gate is open the counter counts the trigger pulses derived from the signal. At the end of the interval the count is displayed, and the cycle is repeated.

Operating Procedure

(1) Set the power switch on.
(2) Apply input signal to channel " A," " B " or " C " input socket.
(3) Select timebase to suit the input signal.
(4) Set function switch to " frequency " and select appropriate channel.
(5) Select display latch in/out.
(6) Set appropriate channel trigger level to suit input waveform.
(7) Set the display time (normally to minimum).
(8) Observe the frequency of the input signal.

NOTE 1—When monitoring low level noisy signals the trigger level controls may have to be readjusted to produce a stable reading.

NOTE 2—"A" channel trigger level is for AC coupling only and will not adjust for amplitude level as per " B " and " C " channel.

4.2—PERIOD AVERAGE MEASUREMENT

PERIOD MODE "A," "B" OR "C"

This mode measures the average value of any decade number of periods of a repetitive input signal as selected by the timebase control. A 10 MHz clock output is applied to the counter. The signal whose period is to be measured is caused to generate repetitive trigger pulses, as in the " frequency " mode, but these are now applied to decade dividers which give a gate time from 1 to 10^8 of the trigger pulses, according to the setting of the timebase/multiplier switches. The counter gate is opened by the first trigger out of the decade divider, and remains open until the preset number of cycles (or periods) have occurred, and a second pulse comes from the divider.
The total count is then displayed in the readout.

Operating Procedure

(1) Set the power switch to on.
(2) Apply the input signal to channel "A," " B " or " C."
(3) Set display latch in/out.
(4) Set function switch to period and select appropriate channel.
(5) Set timebase for the required number of period cycles.
(6) Select display time control to give a suitable display (normally minimum).
(7) The display will indicate the average value of the period of the input signal.

4.3 — TOTALISE MODE A B OR C ÷ N

The totalise mode provides a cumulative count of input " A," " B " or " C." In this mode the internal clock and sample rate oscillator are not used. The input passes through the appropriate trigger circuit and the time base to the gate, and then to the display counter.

The start button switch opens the gate and the stop button switch closes the gate. The display indicates the number of input cycles divided by the time-base/multiplier occurring in the gate time. Accumulative totals may be obtained by successive start/stop sequences.

Operating Procedure

(1) Set the power switch to on.

(2) Set function switch to total ÷ N.

(3) Apply the input signal to channel " A," " B " or " C."

(4) Set the trigger level to suit the input signal.

(5) Set the start slope to trigger on the required edge.

(6) Select the multiplier range on the timebase to provide the required scaler.

(7) Depress the start button to start count.

(8) Depress the stop button to terminate the count.

(9) Depress the reset button to clear display.

4.4—RATIO $\frac{A}{B} \times N$

The frequency ratio mode is identical in function to the frequency measurement mode described in 4.1, but substitutes an external signal for the time reference. The higher of the two frequencies whose ratio is to be measured is normally connected to input "A" and the lower to input "B." Two successive trigger pulses derived from the signal applied to input " B " open and close the counter gate either directly or via dividers.

During the gate open interval the counter counts the trigger pulses derived from input "A" and the ratio $\frac{A}{B} \times N$ is then displayed in the readout.

To obtain higher counts of input " A " for greater resolution, the trigger pulses from input " B " can be divided by selection of the appropriate timebase/multiplier switch.

Operating Procedure

(1) Set the power switch to on.

(2) Set function switch to " ratio $\frac{A}{B} \times N$."

(3) Set the trigger levels to suit the input signal levels.

(4) Set the time-base/multiplier to provide display required.
A = frequency of "A" input.

(5) Observe the ratio $\frac{A}{B} \times N$ where N = number of multipliers.
A = frequency of "A" input.
B = frequency of "B" input.

4.5 TIME INTERVAL B ▶ C

The clock pulses pass via the timebase/divider to the counter. There are two trigger inputs, input " B " and input " C " (or use start and stop push button switches). The control gate is opened by the signal from " B " and closed by the signal from the second " C " and the number of pulses counted gives the time-interval directly. The display indicates the number of prescaled clock cycles occurring during the gate time. Time units are 100ns to 10 seconds per digit.

Operating Procedure

(1) Set the power switch to on.

(2) Apply the start signal to channel " B " input and the stop signal to channel " C " input.

(3) Set function switch to time B▶C.

(4) Set start slope and stop slope switches to + or –ve to provide the required edge of the waveforms to open and close the gate.

(5) Set trigger levels to suit the incoming signal.

(6) Set timebase/multiplier setting to display the required time units.

Note 1— MULTIPLIER TIMEBASE SELECTION

For all normal measurements choose a timebase setting to fill the display without overflow. The resolution can be increased by selecting a high timebase setting. This provides additional digits after the decimal point, as higher timebases are selected and allows the full accuracy of the clock to be utilised. It should be noted, however, that the instrument will be in the " overflow " condition.

Note 2—SETTING THE TRIGGER LEVEL

The trigger level control provides for variation of the point on the waveform at which triggering takes place. For most simple waveforms a zero trigger level is used. However, for pulses, set trigger level to the same polarity as the pulse.

SECTION 5

Technical Description

5.1—INTRODUCTION

The counter timer unit consists of a number of basic circuit blocks (see Fig. 2). All counter timer functions may be produced by interconnecting these basic blocks. A brief description of the blocks is now given.

5.2—INPUT CHANNELS

The input channel amplifiers accept stimuli with a large amplitude and frequency range at a predetermined loading factor. Signal conditioning circuits consisting of high input impedances with overload protection, attenuators and H.F. filters, followed by adjustable hysteresis trigger circuits produce a signal suitable for use in the counter logic. Each channel has a trigger level and slope selection controls to provide optimum counting stability when very low level signals are encountered and to enable + ve and – ve trigger levels to be selected when in timing mode.

5.3—INTERNAL TIME STANDARD

This circuit contains a 10 MHz crystal clock with provision for adjustment of frequency to better than 1 part in 10^6 typically. Thus the clock can be calibrated against a local standard.
The ageing rate is typically 1 PPM per year, but initial ageing may be at a higher rate of 5 parts in 10^7 per month for the initial 6 months operation.
The oscillator is used as the fundamental frequency time reference.
The unit is in a sealed box and breaking the seal will invalidate any warranty.
The unit must be returned to Stanley Laboratories for checking or repair when any doubt arises regarding operation or accuracy.

5.4—TIMEBASE DIVIDER

This circuit receives pulses (via the control logic) from the clock or the input circuits, depending on function, and divides the frequency in selected decades from 1 to 10^8

5.5—GATE TIME GENERATOR

The " gate " circuit that inhibits or enables the display counter is controlled by an edge sensitive bistable circuit such that the first edge opens the gate and the next edge closes the gate. An open/close gate cycle initiates the display time circuitry and inhibits further gate cycles until an internal/external reset occurs.

5.6—RECYCLING OSCILLATOR

This provides sample pulses which may be delayed from $\leqq$ 200ms to $\leqslant$ 5s or held indefinitely. These sample pulses reset the decade dividers of the timebase and display board and also initiate the start of a count sequence. A sample can be triggered by pressing the " reset " button or by contact.

5.7—COUNTING AND DISPLAY

The high speed digital counter counts, within its rated capacity and pulse-pair resolution, every pulse delivered to its input during the interval in which the gate is held open by the counter gating section. The state of the counters is then transferred to a storage register and decoded for the readout.

5.8—CIRCUIT DESCRIPTION AND LAYOUT

The counter timer layout consists of a large main PCB on which all circuits other than counting and display are located. The PCB has its legend split into two areas to facilitate easy location of components.
The counting and display PCB's are a separate assembly screwed to the main PCB and connected by flexible cables. A description of the various circuits now follows.

5.8.1—"A" CHANNEL AMPLIFIER

CIRCUIT DIAGRAM SL483 SHT 1
ASSY SL476 AREA 1

The "A" channel amplifier, contained in a screening box, consists of switchable low pass input filter (SW31, R2, C3) and a 20db attenuator (SW32, R2, C4, R4, C5) with C2 providing AC coupling and D1/D2 protecting the high impedance F.E.T. stage (Q1) from overload voltage.
Q1 drives one input of a wide band differential amplifier M1, the other input being used to remove offsets (RV1) and set the working range of the external trigger level control (RV4) on front panel. The wide band amplifier drives a P.N.P. long tail pair (Q2 and Q3) to provide an output swing sufficient to drive the trigger circuit (Q4 and Q5). Q6 is an edge sensitive pulser providing positive going output pulses. A test button (SW30) feeds 10MHz from the internal oscillator to the input of the "A" channel and disconnects the externally applied signal.
Supplies are +5v and +9v.

" B " AND " C " CHANNEL AMPLIFIERS

CIRCUIT DIAGRAM SL483 SHT 2
ASSY SL476 AREA 2

The " B " and " C " channels are identical and only the " B " channel will be described.
The " B " channel amplifier consists of AC/DC coupling switch (SW29), low pass filter (SW27, R2, C3) and a 20db attenuator SW28 (R3, C4, R4, C5). D1 thru D4 form protection for the high input impedance F.E.T. stage (Q1).
The output from Q1 drives one input side of comparator M, the other side is used for the trigger level voltage derived from RV3. " B " (RV2 on " C " channel) plus a proportion of the comparator output (selected by RV1) giving varying amounts of hysteresis.
The rectangular waveform from M1 is buffered by M3A and inverted by M3B to provide true and complementary outputs, selected by SW3 for feeding to the control logic.
The supplies for this circuit are +5v from the control logic with +12v and −6v derived from zener diodes (ZD1 and ZD2) preceded by full wave bridge D9 thru D12 and energy store C12.
SW26 enables both the " B " and " C " channel amplifiers to be driven from the " B " input socket.

5.8.2—TIMEBASE DIVIDER

CIRCUIT DIAGRAM SL483 SHT 3
ASSY SL476 AREA 3

The 10 MHz internal time standard is buffered by M16D and distributed at normal TTL levels to the first decade of the display counter (M13) via the function switch (SW19) and M12B in the period mode, and to the first decade of the timebase divider chain (M22) via M16B, M10A and M12A, in the frequency and time modes.

The output from the divider chain, selected by SW9 to SW11 and SW12 to SW14 is either buffered by M20D and routed to the first decade of the display counter via SW20 or SW22 and M12B in the time and total modes, or fed via M17A, M12D, M12C to the input of the gate generator (M15A pin 3) in all the other modes.

5.8.3—GATE TIME GENERATOR

CIRCUIT DIAGRAM SL483 SHT 3
ASSY SL476 AREA 3

The gate time generator comprises M15A/B, M17B, M6B, M8A, M8B and M16C. The inputs to initiate a gate time cycle are enabled by M6B pin 6 going high when the display time and reset functions are complete. The first positive transition at M15A pin 3 sets M15A pin 5 high and opens the " gate " via M17B and M8C.

The data input to M15A is now low and the next positive transition sets M15A pin 5 low and closes the " gate," causing a positive transition at M6B pin 11 which starts the display time generator and a negative transition at M4 pin 3 which initiates the internal update/data valid pulse generator. When M6B pin 8 goes low at the end of a gate cycle all inputs to the gate generator are inhibited by M8B pin 6 going low until display time and reset functions are complete.

Alternatively the " gate " may be opened by a positive transition at M15A pin 3 or a low applied to M15A pin 4 (start), and the gate may be closed by a positive transition at M15B pin 11 or a low applied to M15A pin 1 (stop). For very short gates times a pulse stretcher (M7) is used to enable the gate open lamp to be observed by the operator.

5.8.4—RECYCLE OSCILLATOR

CIRCUIT DIAGRAM SL483 SHT 3
ASSY SL476 AREA 3

When M6B pin 8 goes low at the end of a " gate " cycle it turns off Q1 and allows C3 to charge up via R27 and RV1 (display time). When the trigger level of M2B is reached, the negative going edge at its output triggers monostable M1 which discharges C3 fully by turning on Q1 via R32. The negative going edge at the end of the discharge time initiates the pulser formed by C5, R44, R45, M3E and M3B to produce the internal reset signal which clears the display counter, presets the divider chain, and starts another " gate " open/close sequence.

5.8.5—COUNTING AND DISPLAY ASSY

CIRCUIT DIAGRAM SL404
ASSY SL475

NOTE: The display assembly SL475 may be equipped with 4, 6 or 8 counting decades and digits.

Seven decade counters 7490 (M1, 2, 3, 4, 5, 6, 7 on SL 474) feed into seven 4-bit latches (7475) (M8, 9, 10 on SL474) and M1, 2, 3, 4 on SL473. The B.C.D. outputs from the latches, with the first decade B.C.D. from the main P.C.B. assy, are decoded by M11, 12, 13, 14 on SL474 and M5, 6, 7, 8 on SL473 to drive eight (seven segment) digits.

The most significant bit of the most significant decade is linked to the main P.C.B. connecting cable for overflow detection.
R1 thru R8 on SL473 and 474 limit segment and driver transitional currents and R9 thru R12 on SL473 and SL 474 program the segment current (i.e. brightness).

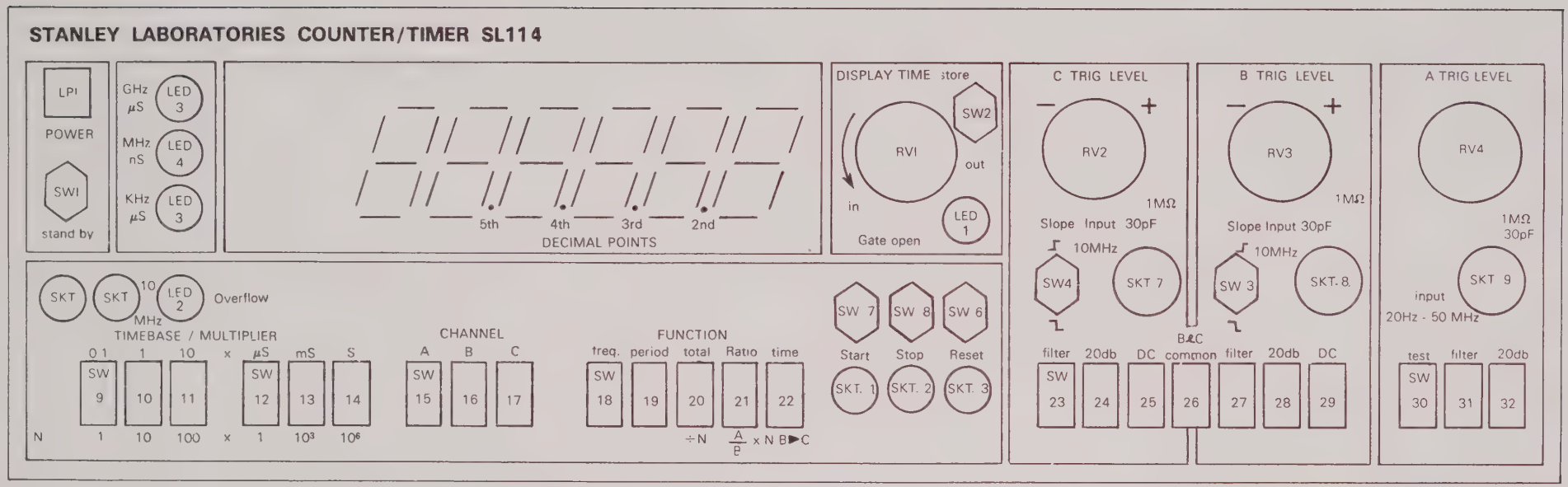
5.8.6—POWER SUPPLIES

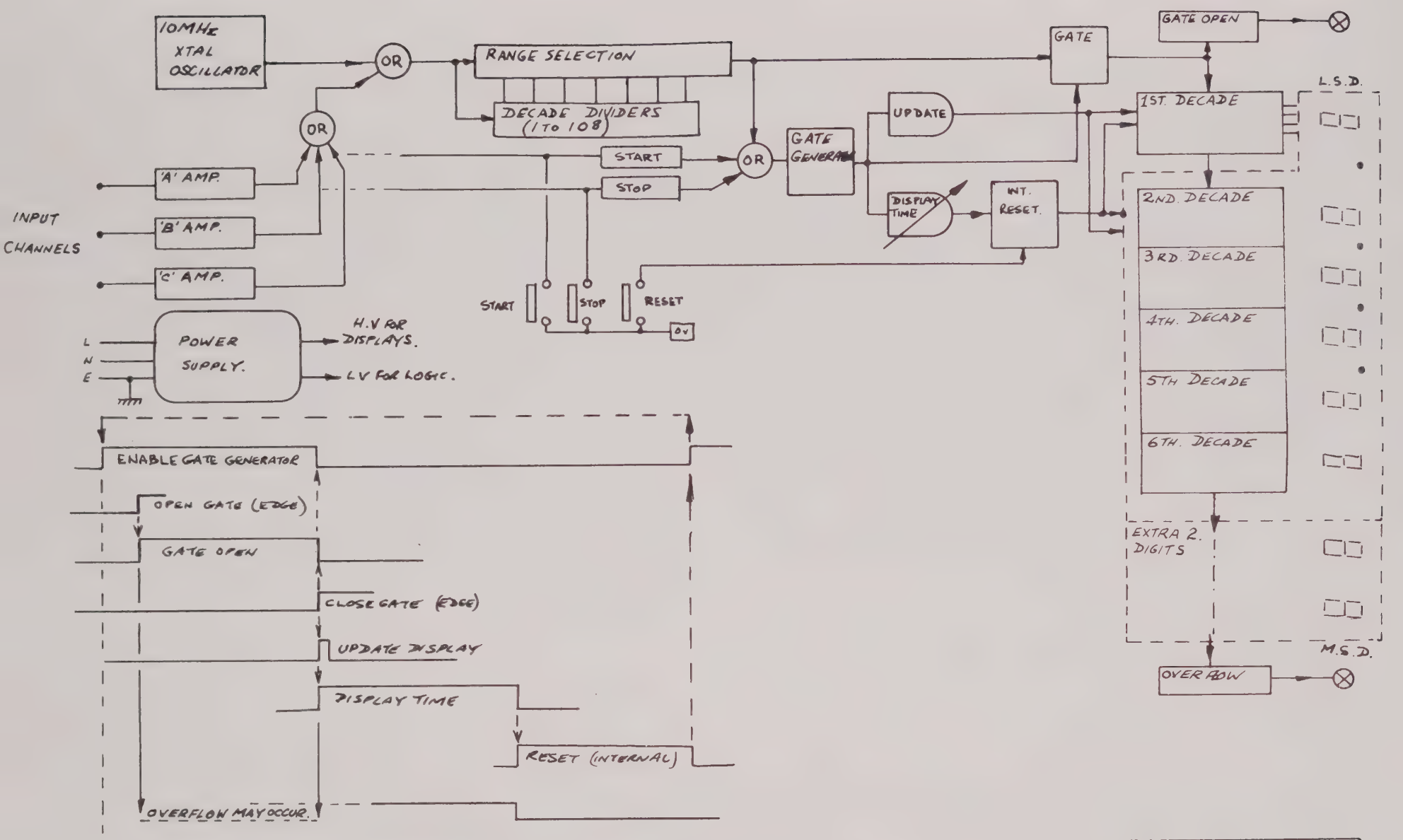
The input supply is fed to the transformer via a 1-amp fuse (240v nominal input) or 2-amp fuse (110v nominal input). The live line is switched (SW1a) by a three-position switch and fed to the primary of the transformer.
The appropriate taps can be soldered for use with 240v input or 110v input. The secondary windings are then fed to the main PCb assembly SL476 to give the required voltage outputs.

The display supply is a high voltage supply nominally 180v and is derived from an emitter follower (03) with ZD1, ZD2 and ZD3 acting as a voltage reference circuit.

The main logic supply is derived from a 5v regulator (reg 2) and is completely s/c proof.

The+9v supply is used to drive the crystal oven and the channel A amplifier Again a 5v regulator is used with its reference set via RV1 to a suitable level of approximately 4v. The supply to the B and C amplifiers is described in 5.8.1.


STANLEY LABORATORIES COUNTER/TIMER SL114
LPI
POWER
SWI
stand by
GHz μS
MHz nS
KHz μS
LED 3
LED 4
LED 3
5th
4th
3rd
2nd
DECIMAL POINTS
DISPLAY TIME store
RVI
SW2
out
in
Gate open
LED 1
C TRIG LEVEL
RV2
1MΩ
Slope Input 30pF
10MHz
SW4
SKT 7
B TRIG LEVEL
RV3
1MΩ
Slope Input 30pF
10MHz
SW 3
SKT. 8.
A TRIG LEVEL
RV4
1MΩ
30pF
input
20Hz - 50 MHz
SKT 9
SKT
SKT
10 MHz
LED 2
Overflow
TIMEBASE / MULTIPLIER
0.1 1 10 x μS mS S
SW 9 10 11 SW 12 13 14
N 1 10 100 x 1 10³ 10⁶
CHANNEL
A B C
SW 15 16 17
FUNCTION
freq. period total Ratio time
SW 18 19 20 21 22
÷N A/B x N B►C
SW 7 SW 8 SW 6
Start Stop Reset
SKT. 1 SKT. 2 SKT. 3
B&C common
filter 20db DC filter 20db DC
SW 23 24 25 26 27 28 29
test filter 20db
SW 30 31 32



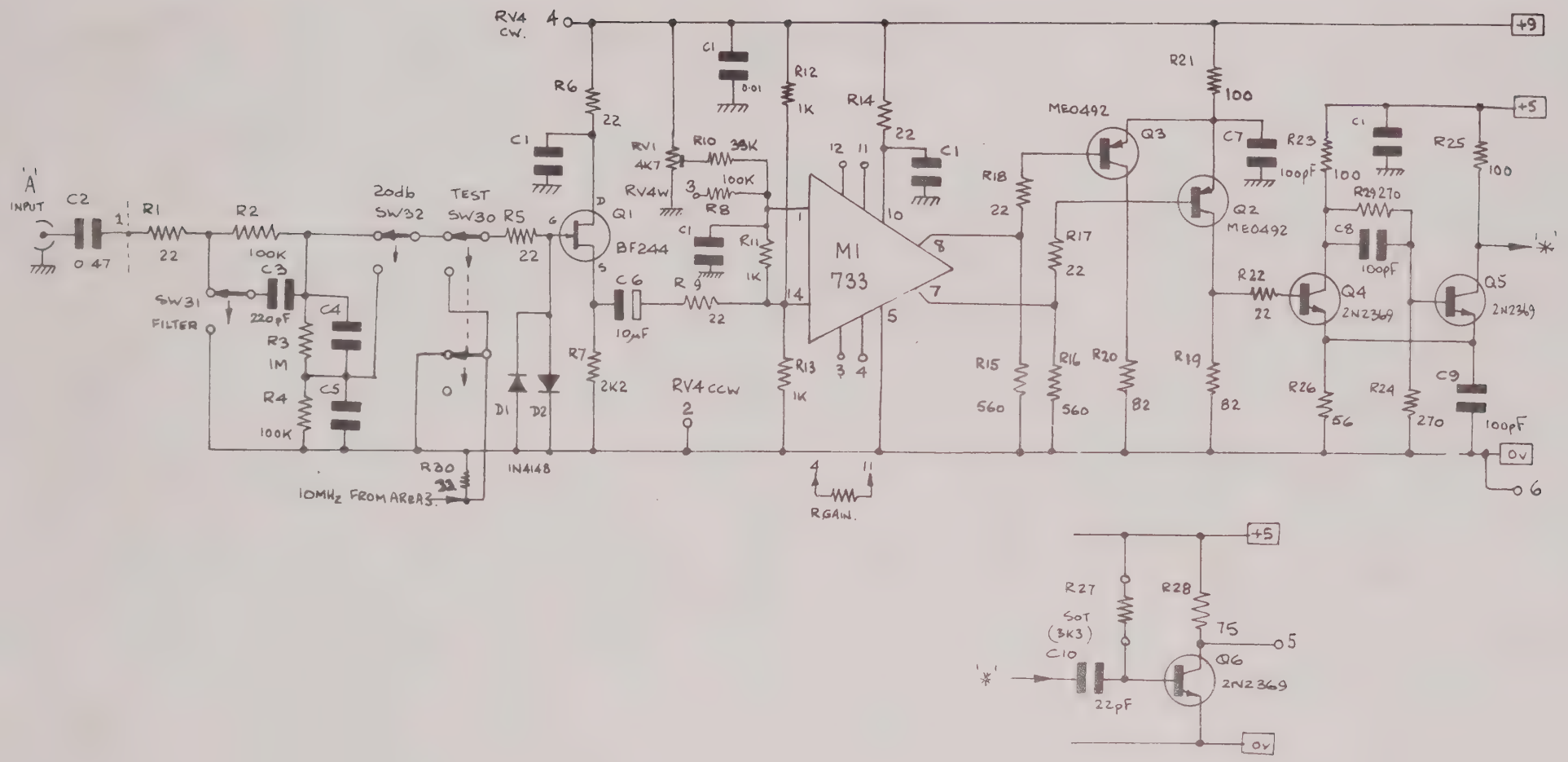
TIMING DIAGRAM NOTE! CORRECT SEQUENCE BUT NOT TO SCALE IN TIME AXIS.

		28-7-75

110 SERIES BLOCK DIAGRAM

	SHT. 1 of 1

H.D.N



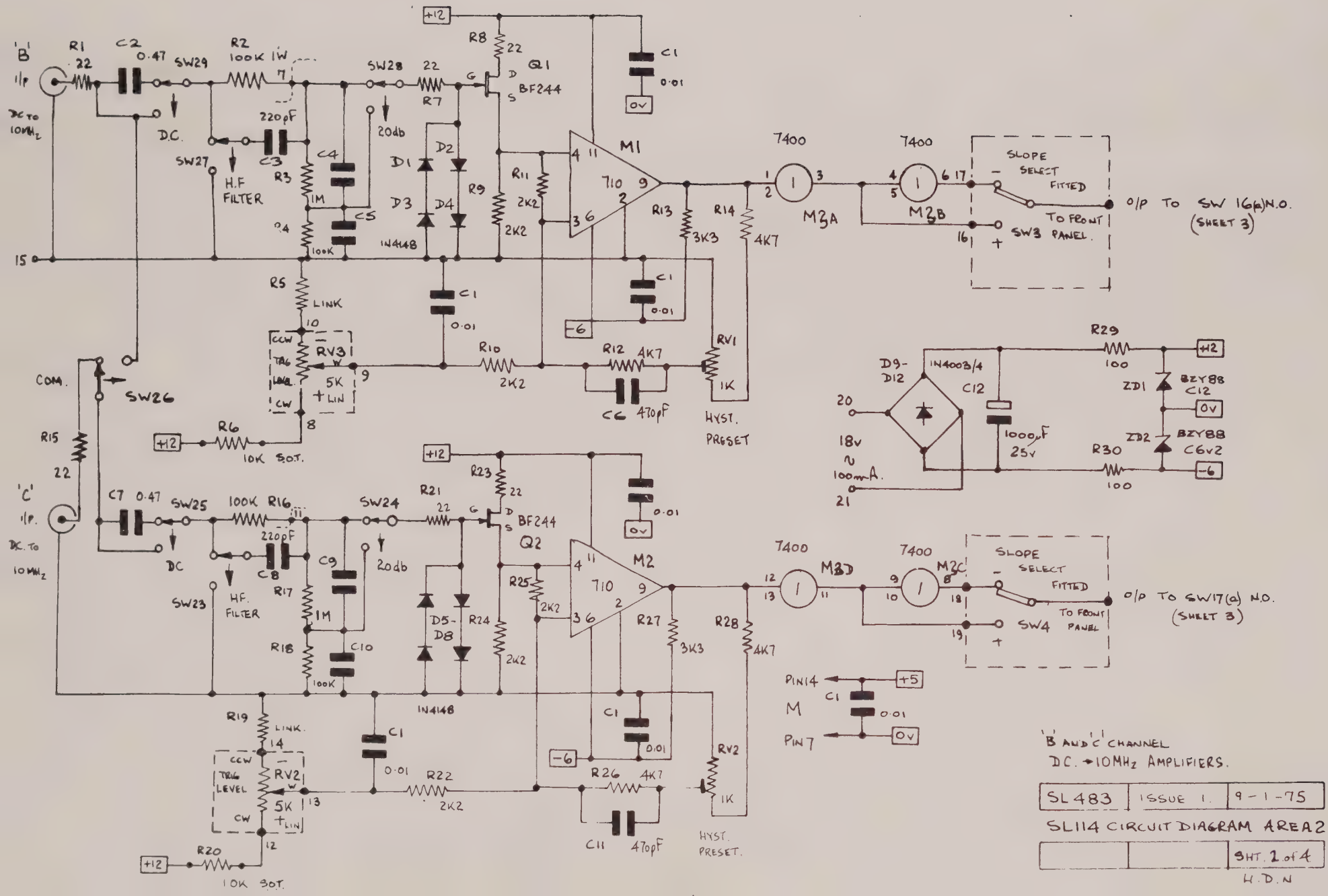
'A' CHANNEL AMPLIFIER.

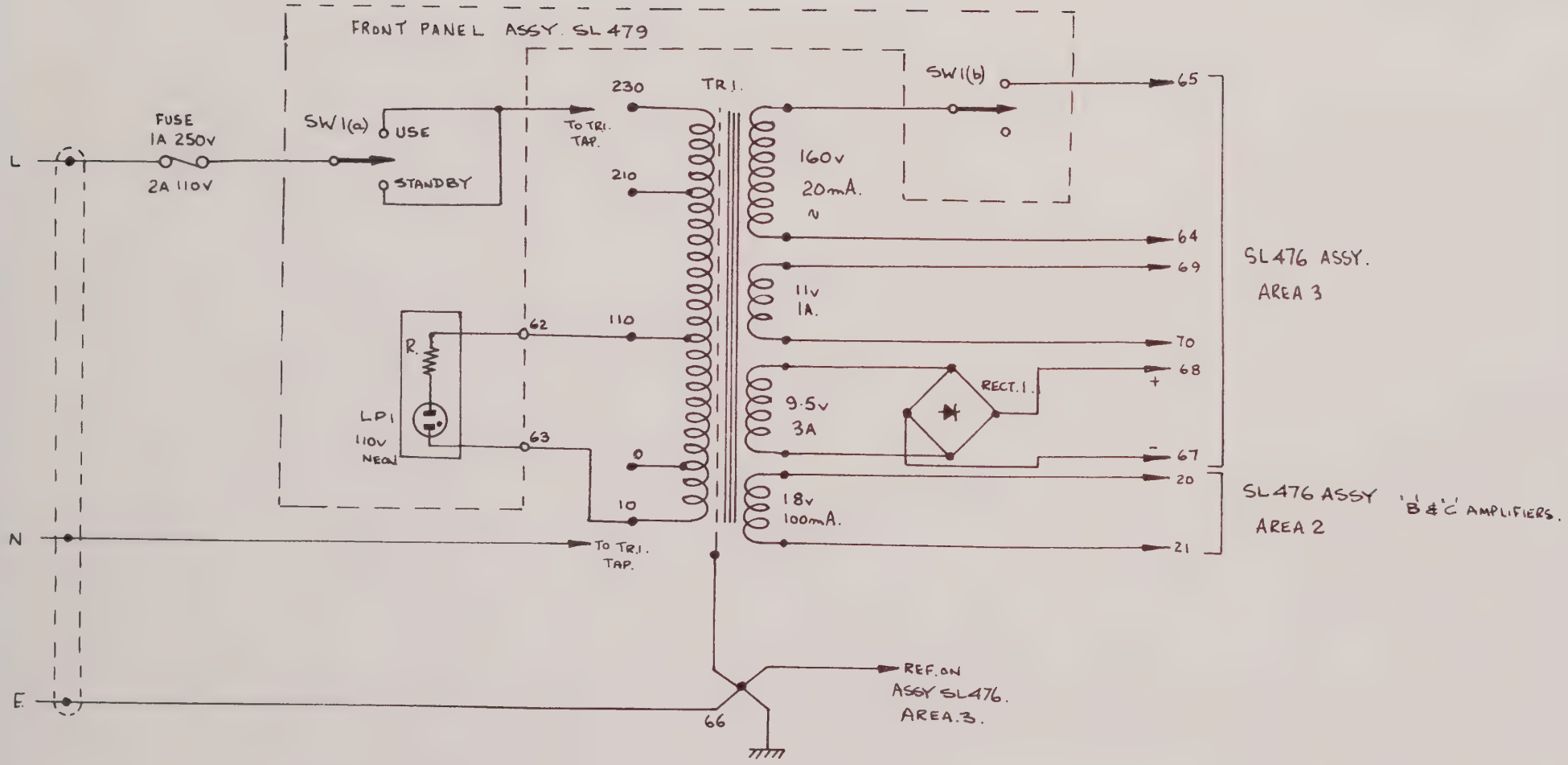
SL 483	1661.	17. 3 75

SL114 CIRCUIT DIAGRAM AREA 1.

	SHT. 1 of 4.

H. D. N.


'B' I/P
DC TO 10MHz
R1 .22
C2 0.47
SW29
R2 100K 1W
SW28
22
R7
R8 22
Q1 BF244
C1 0.01
0V
+12
D.C.
SW27
H.F FILTER
220pF
C3
R3 1M
C4
C5 0.1
100K
20db
D1
D2
D3
D4
IN4148
R9
R11 2K2
2K2
M1
710
4 11
3 6
2
9
R13 3K3
R14 4K7
7400
M3A
M3B
SLOPE SELECT FITTED
TO FRONT PANEL
SW3
O/P TO SW 16(a) N.O. (SHEET 3)
15
R5 LINK
10
CCW TRG LVL CW
RV3 5K +LIN
9
8
R6 10K 5OT.
R10 2K2
R12 4K7
RV1 1K
C6 470pF
HYST. PRESET
-6
COM.
SW26
R15 22
'C' I/P.
DC. TO 10MHz
C7 0.47
SW25
100K R16
SW24
R21 22
R23 22
Q2 BF244
M2
M3D
M3C
SW23
HF. FILTER
220pF
C8
C9
R17 1M
R18 100K
C10
R24
R25 2K2
R27 3K3
R28 4K7
SW4
O/P TO SW17(a) N.O. (SHEET 3)
PIN14
M
PIN7
+5
R19 LINK
14
CCW TRIG LEVEL CW
RV2 5K +LIN
13
12
R20 10K 5OT.
R22 2K2
R26 4K7
RV2 1K
C11 470pF
HYST. PRESET.
D5-D8
IN4003/4
D9-D12
C12 1000μF 25V
20
18V ~ 100mA.
21
R29 100
R30 100
ZD1 BZY88 C12
ZD2 BZY88 C6V2
'B' AND 'C' CHANNEL
DC → 10MHz AMPLIFIERS.
SL 483
ISSUE 1.
9-1-75
SL114 CIRCUIT DIAGRAM AREA 2.
SHT. 2 of 4
H.D.N



REAR PANEL ASSY 480
POWER TRANSFORMER CONNECTIONS

SL483	ISS. 1.	17. 3. 75

SL114 CIRCUIT DIAGRAM AREA 3

	SHT 4 of 4

A SW15 (a) B SW16 (a) C SW17 (a)

COUNT INPUT (1ST SELECTION).

FREQ SW18 (a) PERIOD SW19 (a) TOTAL SW20 (a) RAT SW

INPUT AMPLIFIERS.
A 50MHz
B 10MHz
C 10MHz
REF. ONLY

10MHz XTAL OSC 1
LINK 46 47
R1 1K
SKT.4.
R2 100
10MHz
3 REF. ONLY. 2 4
+5 0V +5 0V 51
0V SKT.5.

M16D

R17 1K
C10 10MHz
To 'A' CHANNEL 'TEST'.
47pF

DIVIDER INPUT

M11B
C S
D R
74H74

M30A M30B

M12A
74S00

M22 ÷10 50MHz 74196
M28 ÷10 7490
M27 ÷10 50MHz 74196
M26 ÷10 7490
M23 ÷10 7490
M21 ÷10 7490
M19 ÷10 7490
M18 ÷10 7490

M29D
M29A
M25C
M29C
M29B

SET '0'/N
SET '9'/N

SW9 (a) SW10 (a) SW11 (a) SW12 (a) SW13 (a) SW14 (a)

STOP 7
TIME/P
TOTAL/N
START 7
TIME/N

WAIT/N

FREQ
R3 4K7
SW18 (b)
D1 IN4148
FREQ/P

PERIOD
R4 4K7
R5 4K7
SW19 (b)
D2 IN4148
PERIOD/P

TOTAL
R6 4K7
SW20 (b)
TOTAL TIME/P

RATIO
R7 4K7
SW21 (b)
RATIO/P

TIME
R8 4K7
R9 4K7
SW22 (b)

M16B
M20B
74S00
M10A
74S20
M25B
M25D
M25A
M16A

PERIOD/P
FREQ/P
R10 4K7
SW11 (b)
R11 4K7
SW10 (b)
R12 4K7
SW9 (b)
R13 220
55

M32B M32A M32C M32D M31A M31C M31D M31B M30C M30D
M24.
74141
M5E 7405 o/c
M20A 74S00

R13 100K 5TH DISPLAY ASSY 12
R14 100K 4TH 11
DECIMAL POINT DRIVE
R15 100K 3RD 10
R16 100K 2ND 9
0V
4 LINES

KHz/μSec. MHz/μSec. GHz/μSec.
LED.3. LED.4. LED.5
SW14 (b) SW13 (b) SW12 (b)

DECIMAL POINT POSITION FOR B.C.D. OUTPUT OPTION. 58.59.60.61.

+ 68
C11 5x1000μF.
REG.1. LM309K
C12 0.1
Note. REG1&2 on heat sink.
+5V LOGIC 14
D.C. FROM RECT.
67 −
66 SCR's EARTH & FRONT PANEL
D9-D12 IN4003/4
69
11v. 1A ~
70
C13 3x1000μF
REG2 LM309K
C14 0.1
R50 470
RV1
RFC.1.
+9v OSC & AMP.
C19 1000μF. 25v
SET +9v
470
C1
65
160v ~ (SWITCHED) 64
D13 IN4006
C15 0.8μF 250
MJE340 Q3
R52 2K2
R51 6K8
ZD1 62v ZD2 62v ZD3 62v
+180v DISPLAY 19
0v 13
C16 10μF 250
R53 2K2
−180v DISPLAY. 18
D14 IN4006

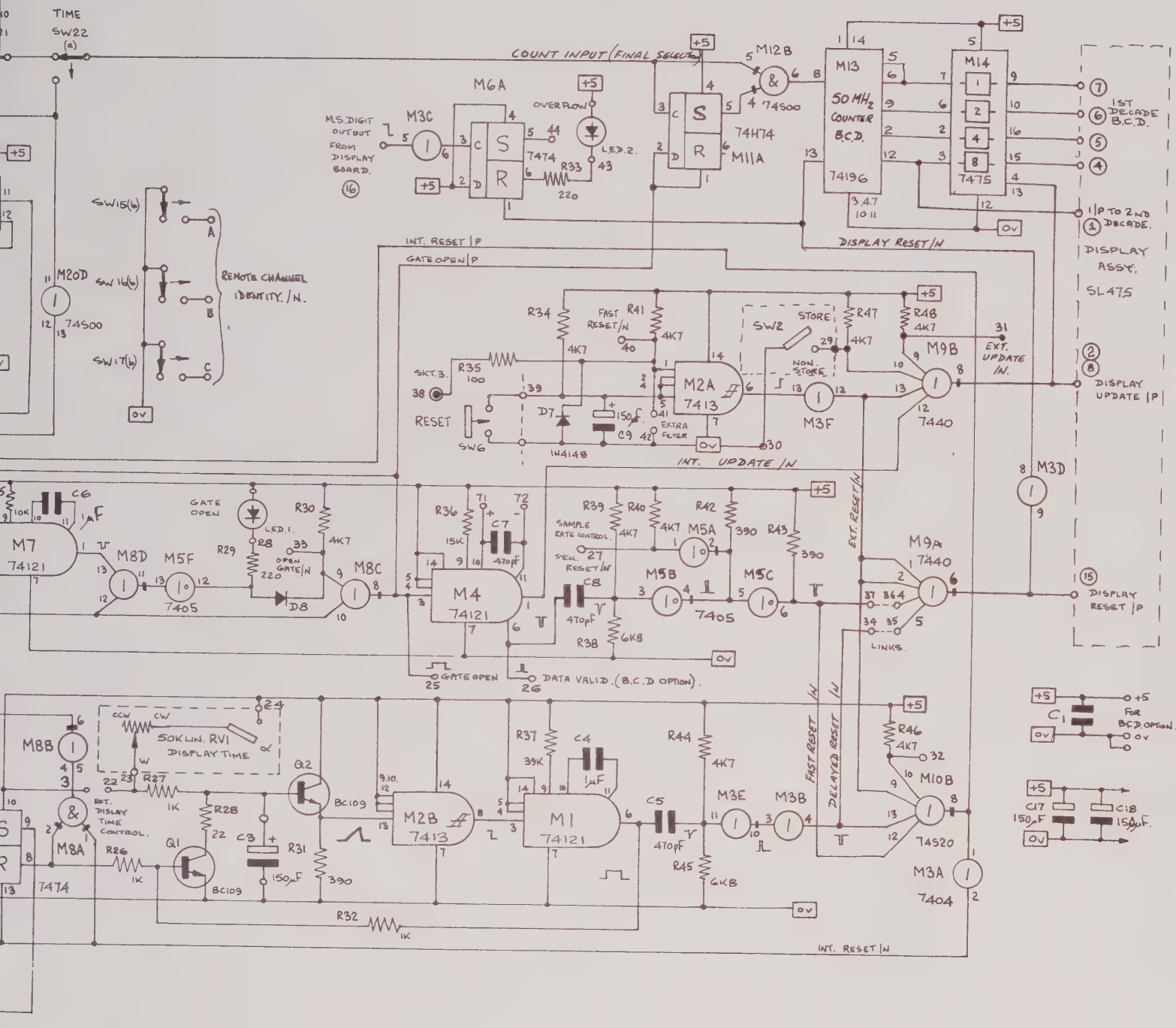
M20C M12D M17A 74S10 74S00
M12C M17C 74S10 74S00
M15A 74H74
M16C
M15B 74S10
M17B 74S10
M6B
74H74

R22 4K7
SW14 (a)
57 LINK 58
SKT.1.
R24 100 START
SW7
D6 IN4148
52 51
0V
+5
R23 4K7
R49 4K7
54

SW8 49 50
STOP
SKT.2
R20 100
D3 IN4148
D4 IN4148
D5 IN4148
0V

TIME/N

M5D 7405



SL483	ISS.1.	15-1-75
SL114 CIRCUIT DIAGRAM (AREA 3)		
		SHT 3 of 4

H.D.N.

DIGIT N° (LH) | 8 | 7 | 6 | 5 | 4 | 3

M4 7475 | M3 7475 | M2 7475

M8 DD700 OR DM8880 | M7 DD700 OR DM8880 | M6 DD700 OR DM8880

R12 | R11 | R10 | R8 | R4 | R7 | R3 | R6 | R2

KA e d c b a g f DP. A

f g e KA d A c DP b a

M14 DD700 OR DM8880 | M13 DD700 OR DM8880 | M12 DD700 OR DM8880

R12 | R4 | R8 | R11 | R3 | R7

BCD

M10 7475 | M9 7475 | M8 7475

M7 7490 | M6 7490 | M5 7490 | M4 7490 | M3 7490 | M2 7490

(N) = CONNECTOR ROW FOR SL115 INPUT.

8 7 6 5 4 3 2 1

D.P. DECADE POSITIONS. (RH. PLACEMENT.)

M.S. DECADE OUTPUT 4, 6 or 8 DIGITS. SEE LINKS

ASSY 474 iss 1.

SL 404 8 DIGIT DISPLAY CIRCUIT DIAGRAM OF COMPLETE ASSY. SL 475

2 1 R.H

M1 7475

C1 0.0 (5 PLACES)

BCD R9

M5 DD700 OR. DM8880

R5 R1

KA e d c b a g f DP A

ASSY 473 iss 1

ASSY 472 iss 1.

DP b a

f g e KA d A c DP b a

R5 R1

R10 R2 R6 R9

M11 DD700 OR. DM8880.

BCD BCD.

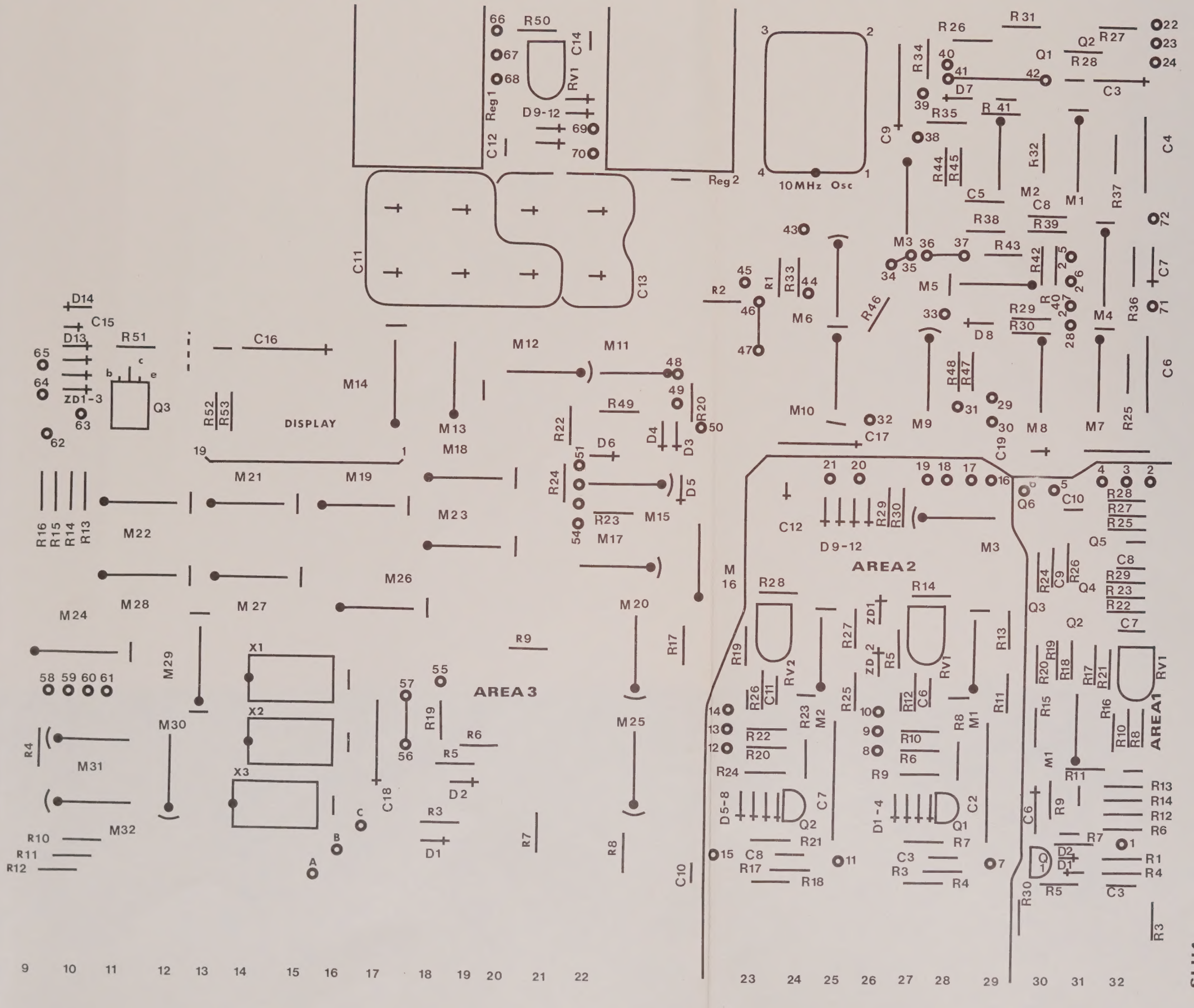
M1 7490

C1 11 PLACES

RESET/P INPUT 2ND DECADE UPDATE/P D (8) C' (4) B (2) A (1) B.C.D. FOR 1ST DECADE +5V 0 +180 -180

ISING 472, 473, 474. Assy's.

H.D. N 8/1/75


AREA 1
AREA 2
AREA 3
DISPLAY
10MHz Osc
Reg 1
Reg 2
SLII4

MP MASTER
MA24467